AMENDMENTS TO THE CLAIMS

1. (Currently Amended) A synchronization circuit for receiving an input signal and a clock having a frequency which is equal to a transfer rate of the input signal, and synchronizing the input signal with the clock, said circuit comprising:

a state detection circuit for receiving the input signal and the clock, and outputting a control signal according to the temporal relationship between a transition point of the input signal and an edge of the clock;

a delay selection circuit for receiving the input signal and the control signal outputted from said state detection circuit, adding a delay to the input signal on the basis of the control signal, and outputting an output signal; and

a latch circuit for receiving the clock and the output signal outputted from said delay selection circuit, synchronizing the output signal outputted from ~~the~~ said delay selection circuit with the clock~~,~~ and outputting the synchronized signal.

2. (Currently Amended) A synchronization circuit for receiving an input signal and a clock having a frequency which is equal to a transfer rate of the input signal, and synchronizing the input signal with the clock, said circuit comprising:

a state detection circuit for outputting a control signal according to the temporal relationship between a transition point of the input signal and an edge of the clock;

a delay selection circuit for adding a delay to the clock on the basis of the control signal; and

a latch circuit for synchronizing the input signal with the clock outputted from ~~the~~ said delay selection circuit, and outputting the synchronized signal.

3. (Currently Amended) A synchronization circuit for receiving plural input signals having phases which are irrelevant to each other~~,~~ and a clock having a frequency which is equal to a transfer rate of the plural input signals, and synchronizing the plural input signals with the clock, said circuit comprising:

a state detection circuit for outputting control signals relating to the respective input signals, according to the temporal relationship between transition points of the plural input signals;

a delay selection circuit for adding delays to the respective input signals on the basis of the control signals relating to the respective input signals; and

a latch circuit for synchronizing the respective signals outputted from ~~the~~ said delay selection circuit with the clock, and outputting the synchronized signals.

4. (Currently Amended) A synchronization circuit for receiving plural signal bundles each comprising a set of plural input signals which are synchronized with each other and a single clock having a frequency which is equal to a transfer rate of the plural input signals, in which the phases of the input signals included in one signal bundle are irrelevant to the phases of the input signals included in the other signal bundles, and for synchronizing the input signals included in one signal bundle with the input signals included in the other signal bundles by using a single synchronization clock that is selected from among the clocks included in the respective signal bundles, said circuit comprising:

a state detection circuit for detecting the state between the plural input signals included in the respective signal bundles;

a clock selection circuit for receiving the clocks included in the respective signal bundles, and selecting one of the inputted clocks, as a synchronization clock, on the basis of the result of the state detection performed between the respective signal bundles by ~~the~~ said state detection circuit;

a delay selection circuit for adding delays to the plural input signals included in each signal bundle, on the basis of the result of the state detection performed between the respective signal bundles by said state detection circuit; and

a latch circuit for synchronizing the output signal from ~~the~~ said delay selection circuit for each signal bundle, with the selected synchronization clock, and outputting the synchronized signal.

5. (Currently Amended) A synchronization circuit as defined in Claim 4, wherein said state detection circuit comprises:

an early/late detection circuit for detecting which signal bundle is earlier in input timing between the respective signal bundles, and outputting an early/late detection signal; and

an overlap detection circuit for detecting an overlap period between the respective signal bundles, and outputting an overlap detection signal;

wherein said clock selection circuit ~~selects~~is operable to seltect, as a synchronization clock, a clock included in a signal bundle which is determined as being

inputted earlier between the respective signal bundles, on the basis of the early/late detection signal; and

said delay selection circuit ~~adds~~ is operable to add delays based on the early/late detection signal and the overlap detection signal, to the plural input signals included in the respective signal bundles.

6. (Currently Amended) A synchronization circuit as defined in Claim 1, wherein said delay selection circuit comprises:

a delay circuit for adding a delay to the input signal; and

a selection circuit for selecting either the input signal or the output signal of ~~the~~ said delay circuit on the basis of the control signal.

7. (Currently Amended) A synchronization circuit as defined in Claim 2, wherein said delay selection circuit comprises:

a delay circuit for adding a delay to the inputted clock; and

a selection circuit for selecting either the inputted clock or the clock outputted from ~~the~~ said delay circuit on the basis of the control signal.

8. (Currently Amended) A synchronization circuit as defined in Claim 3, wherein said delay selection circuit comprises:

a delay circuit for adding delays to the respective input signals; and

a selection circuit for selecting one signal from among the plural input signals and the signals outputted from ~~the~~ said delay circuit, for each of the plural input signals, on

the basis of the control signals relating to the respective input signals, and outputting the selected one signal.

9. (Currently Amended) A synchronization circuit as defined in Claim 1, wherein said state detection circuit ~~detects~~ is operable to detect the state of the input signal on the basis of ~~a~~an externally supplied preamble detection signal which ~~is supplied from the outside and~~ indicates the positional relationship of data to be synchronized.

10. (Currently Amended) A synchronization circuit as defined in Claim 2, wherein said state detection circuit ~~detects~~ is operable to detect the state of the input signal on the basis of ~~a~~ an externally supplied preamble detection signal which ~~is supplied from the outside and~~ indicates the positional relationship of data to be synchronized.

11. (Currently Amended) A synchronization circuit as defined in Claim 3, wherein said state detection circuit ~~detects~~ is operable to detect the state of the input signal on the basis of ~~a~~ an externally supplied preamble detection signal which ~~is supplied from the outside and~~ indicates the positional relationship of data to be synchronized.

12. (Currently Amended) A synchronization circuit as defined in Claim 4, wherein said state detection circuit ~~detects~~ is operable to detect the state of the input signal on the basis of ~~a~~ an externally supplied preamble detection signal which ~~is supplied from the outside and~~ indicates the positional relationship of data to be synchronized.

13. (New) A synchronization circuit as defined in Claim 1, wherein said delay selection circuit is operable to add a delay to the input signal on the basis of the control signal without utilizing the clock.